Statistical Logic Cell Delay Analysis Using a Current-based Model

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Abstract

A statistical model for the purpose of logic cell timing analysis in the presence of process variations is presented. A new current-based cell delay model is utilized, which can accurately compute the output waveform for input waveforms of arbitrary shapes subjected to noise. The cell parasitic capacitances are pre-characterized by lookup tables to improve the accuracy. To capture the effect of process parameter variations on the cell behavior, the output voltage waveform of logic cells is modeled by a stochastic Markovian process in which the voltage value probability distribution at each time instance is computed from that of the previous time instance. Next the probability distribution of $\alpha\%V_{dd}$ crossing time, i.e., the hitting time of the output voltage stochastic process is computed. Experimental results demonstrate the high accuracy of our cell delay model compared to Monte-Carlo-based SPICE simulations.

Categories and Subject Descriptors: B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

General Terms

Algorithms, Measurement, Performance, Design, Reliability

Keywords

Statistical gate timing analysis, Crosstalk noise, Process variations

1. Introduction

The downscaling of process technologies to 90nm and below results in a significant increase in the device and interconnect manufacturing process variations of VLSI circuits. These effects can produce excessive timing uncertainty, which in turn requires sophisticated timing analysis techniques and tools to reduce the uncertainty. As the number of sources of variations increases, corner-based static timing analysis (STA) techniques computationally become very expensive. Moreover, with decreasing size of transistors and interconnect width, the variation of electrical characteristics is getting proportionally higher. The process corner approach, which used to work well, may thus result in inaccurate estimates and suboptimal designs. Statistical static timing analysis (SSTA) has been used to address the above-mentioned shortcoming of the STA.

The fact that the interconnect delay may dominate the cell delay in modern VLSI circuits has drawn attention toward producing faster and more accurate interconnect delay models. However, the conventional logic cell delay models have not improved as much. They generally use the concept of voltage-based cell delay modeling, meaning the cell is pre-characterized with 2-D lookup tables with input slew and output load as the keys to the tables and the output slew and gate delay as the output of the tables. These look-up tables are inherently incompatible with the arbitrary shapes of a noise-affected input waveform, and hence, fall apart in processing noisy inputs.

Current-based logic cell delay modeling has been introduced as an alternative approach to cope with the shortcomings of the conventional approaches. Authors in [1] describe a current-based model in which a pre-characterized current source is utilized. They model the parasitics of the logic cell with a single constant capacitance at the output node. The parasitic effects are not modeled accurately in [1] e.g., the Miller and input parasitic effects are ignored. Keller et al in [2] present the most recent and accurate current-based model (referred to as KTV, for Keller, Tseng, and Verghese, throughout this paper) in handling noisy waveforms of arbitrary shapes. Similar to [1], a pre-characterized current source is used. The parasitic components, namely the Miller and the output capacitances, are assumed to be constant regardless of the input and output voltage values. Based on our observation, these capacitive effects can vary significantly depending on cell input and output voltages. The assumption of fixed values can give rise to large inaccuracy especially for complex cells. Furthermore, this model does not address the effect of process variations. On the other hand, the existing statistical gate-delay models such as [3] and [4] rely on the conventional voltage-based cell delay modeling. This class of gate delay modeling approaches cannot handle the noisy input waveforms accurately. Therefore, the statistical gate delay analysis is restricted to noiseless ramp input.

The objective of the present work is to devise an accurate statistical logic cell delay model to handle noisy inputs in the presence of process variations. The existing cell delay analysis techniques either do not accurately model the parasitic and non-linear behavior of logic cells or do not handle the process variations properly. To address the first weakness, a new current-based model in which the cell parasitics are pre-characterized as a function of the input and the output voltage values is presented. To address the second shortcoming, a mathematical method is presented whereby first the sensitivities of cell model elements with respect to the sources of variation are characterized. The output voltage is then represented by a stochastic Markovian process. Finally, using the probability distribution of output voltage values at each time instance, the distribution of $\alpha\%V_{dd}$ crossing time of the output voltage is accurately calculated.

The remainder of this paper is organized as follows. In section 2 our current-based logic cell circuit model is described. Section 3 describes our statistical approach to consider process variations effects. Section 4 and 5 explain the experimental results and conclusions respectively.

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2. Current-based Cell Delay Modeling

The main motivation for us to create a new model is that the existing current-based models sometimes exhibit rather large errors compared to SPICE. It is crucial to use a highly accurate circuit model for considering the effect of process variations because the circuit model error may dominate the error of ignoring process variations. In such a case the analysis would not benefit from consideration of process variations.

2.1 The proposed cell delay model

Our model shown in Figure 1 comprises of two main components, namely, 1) parasitic capacitances to model the parasitic behavior at input and output nodes and the Miller effect between the nodes, and 2) a current source at the output node to model the nonlinear behavior of the logic cell. Each component is a function of the input and output voltages. As a result, the proposed cell model is represented by the following KCL equation:

$$i_o + I(V_i,V_o) + \left(C_o(V_i,V_o) + C_M(V_i,V_o)\right)\frac{\Delta V_o}{\Delta t} - C_M(V_i,V_o)\frac{\Delta V_i}{\Delta t} = 0 \qquad (1)$$

$I(V_i,V_o)$ is determined for each logic cell by sweeping the DC values of input and output voltages and measuring the current sourced by the cell output pin in SPICE. A 2-D lookup table is constructed to store $I(V_i,V_o)$ values. In addition, $C_M(V_i,V_o)$ and $C_o(V_i,V_o)$ values are also characterized through a series of SPICE-based transient simulations, where saturated ramp input and output voltages are applied to the input and/or output nodes and output current is monitored. 2-D lookup tables are used to store $C_M(V_i,V_o)$ and $C_o(V_i,V_o)$ values.

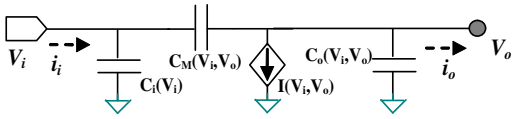

Figure 1. Our proposed current-based circuit model of a logic cell.

Precise estimation of the output load is crucial for accurate delay calculation of a logic cell. The input parasitic capacitances of fan-out cells should be considered as part of the load for delay calculation of the driver cell. A transient analysis based on Equation (2) is used to determine C_i.

$$i_i = \left(C_i(V_i,V_o) + C_M(V_i,V_o)\right)\frac{\Delta V_i}{\Delta t} - C_M(V_i,V_o)\frac{\Delta V_o}{\Delta t} \qquad (2)$$

Although C_i is in fact a function of the input and output voltage values, in practice an input-voltage-dependent C_i is all that can be efficiently utilized. This is because when calculating the delay of a logic cell, the output voltage values of its fanout cells are unknown. Equation (1) can be rewritten by substituting the output current, i_o, as a function of the output load and output voltage. Arbitrary (e.g., RLC) loads can be handled by our model; however, without loss of generality, we consider a capacitive load, C_L from here on to simplify the presentation:

$$C_L\frac{\Delta V_o}{\Delta t} + C_o\frac{\Delta V_o}{\Delta t} + I(V_i,V_o) + C_M\frac{\Delta V_o}{\Delta t} - C_M\frac{\Delta V_i}{\Delta t} = 0 \qquad (3)$$

Equation (3) can be rewritten w.r.t to output voltage values:

$$V_o(t_{k+1}) = V_o(t_k) + \frac{1}{C_L + C_o + C_M} \times \left(C_M(V_i(t_{k+1}) - V_i(t_k)) - I(V_i,V_o) \times \Delta t\right) \qquad (4)$$

3. Proposed Statistical Cell Delay Model

As stated earlier, it is essential to account for the variations of physical parameters in the logic cell model. In this paper we consider L_{int}, V_{TH0}, T_{OX}, and W_{int} as the physical parameters of interest. The logic cell elements (i.e., the current source and capacitive parasitics) are represented as a function of physical parameters of the cell to capture the process variations. More precisely, a first order (FO) model [5] is utilized to express any logic cell element E as a function of the physical parameters:

$$E = e_0 + e_1 \cdot \Delta X_1 + \ldots + e_m \cdot \Delta X_m \qquad (5)$$

Here, e_o is the nominal value of E whereas e_i is the sensitivity coefficient of element E with respect to physical parameter X_i. ΔX_i is the variation of X_i and m denotes the number of sources of variation. We assume that X_i's have independent Gaussian probability distributions. (Parameter distribution independence can be achieved by principal component analysis (PCA) [6],[7].) By using the best mean squared error fit, e_i's are derived from a series of Monte-Carlo-based SPICE simulations. These sensitivity values are stored in 2-D look-up tables (c.f. Figure 2.)

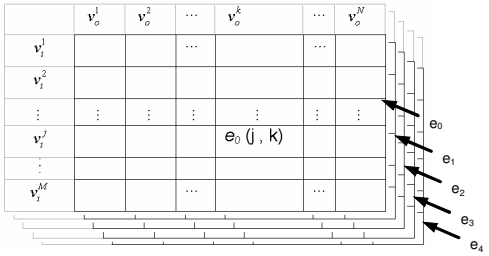

Figure 2. The sensitivity-based look-up tables to model a physical parameter variation.

Equation (4) shows how to compute the output voltage when the cell is operating under the nominal condition. By applying random variables associated with each cell element, this equation can be utilized to express the output voltage waveform distribution in the presence of process variations as detailed next. We define Stochastic First Order (*SFO*) modeling form of a signal waveform W(t) as an ordered set of N FO expressions f_i (i=1…N) where f_i gives the variational linear form of $W(t_i)$ and t_i denotes the i^{th} sampling point. A SSTA calculator propagates the SFO form of the voltage waveforms at the primary inputs throughout the circuit in linear-time in the circuit size. The key task is thus how to propagate the SFO at the input of a logic gate, $\{f_k\}$, to its output node (adopting the single input change model), thus calculating the SFO of the output voltage waveform, $\{g_k\}$. To do this, we utilize Equation (4) as follows:

$$g_{k+1} = g_k + \frac{C_M\left(f_{k+1} - f_k\right) - h_{k+1} \cdot \Delta t}{C_L + C_o + C_M} \cong g_{k+1,0} + \sum_{j=1}^{m} g_{k+1,j} \cdot \Delta X_j \qquad (6)$$

where h_{k+1} denotes the FO form of current source of Figure 1 as looked up by the nominal values of f_{k+1} and g_k. Notice that C_o and C_M are in the FO forms. In addition, C_L has been cast into the FO form. The right hand side of Equation (6) exploits the fact that the division, multiplication and summation of FO expressions can be performed and the result cast into a FO form. For example, this may be approximately done by linearization with respect to X_i's based on Taylor series expansion.

Equation (4) can be used recursively, meaning that the output voltage at each time instance can be written as a linear function of the sources of variation. Therefore, $V_o(t_i)$ which is the summation of the normal distributions of process parameters is modeled by a normal distribution. The fact that the distribution of the output voltage at each time instance can be computed from that at the previous time instance leads us to the concept of a stochastic Markovian process [8] as explained next.

Definition 1: A stochastic process $x(t)$ is called a Markovian process if the following is satisfied for every n and $t_1<t_2<\ldots<t_n$:

$$P\left(X(t_n) \le x_n \mid X(t_1),...,X(t_{n-1})\right) = P\left(X(t_n) \le x_n \mid X(t_{n-1})\right) \quad (7)$$

$V_o(t)$ is a Markovian stochastic process. We use this property to compute the distribution of any $\alpha\%V_{dd}$ crossing time of $V_o(t)$.

3.1 Computing the delay distribution

As stated earlier, the current-based cell model enables one to compute the output voltage distribution at each time instance. However, the problem of interest is to compute the distribution of the delay or in general the distribution of any $\alpha\%V_{dd}$ crossing time of the output voltage. For simplicity we normalize V_o with respect to V_{dd}. The problem can be stated as follows.

***Problem Statement*:** Given the stochastic Markovian process $V_o(t_i)$, calculate the *hitting time* probability (defined as follows:)

$$P(T_\alpha \le t_n) \text{ where } T_\alpha = \inf\{t_i : V_o(t_i) = \alpha\} \quad (8)$$

By definition T_α is the *first time* that process V_o reaches the value of α. The hitting time probability in Equation (8) is used to characterize the distribution of any $\alpha\%$ crossing time of the output voltage. By finding the hitting probability, we compute the cell delay distribution in the presence of the process variations.

***Lemma* 1**: For a Markovian process $X(t_i)$,

$$P\left(X(t_n) < \alpha \mid X(t_1) < \alpha,..., X(t_{n-1}) < \alpha\right) = P\left(X(t_n) < \alpha \mid X(t_{n-1}) < \alpha\right)$$

This lemma follows from the Markovian process property.

***Theorem* 1:** The hitting time probability for the Markovian process $V_o(t_i)$ is computed as follows:

$$P(T_\alpha \le t_n) = 1 - \Lambda \quad \text{where}$$

$$\Lambda = \begin{cases} \dfrac{\prod_{i=2}^{n} P\left(V(t_i) < \alpha \wedge V(t_{i-1}) < \alpha\right)}{\prod_{i=2}^{n-1} P\left(V(t_i) < \alpha\right)} & \text{if } \forall i : P\left(V(t_i) < \alpha\right) \neq 0 \\ 0 & \text{otherwise} \end{cases} \quad (9)$$

***Proof*:** $P(T_\alpha \le t_n) = 1 - P(T_\alpha > t_n)$. Without loss of generality, we assume that the output voltage is making a low to high signal transition. Therefore, the event $(T_\alpha > t_n)$ is equivalent to the joint event $(V(t_1) < \alpha \wedge V(t_2) < \alpha \wedge ... \wedge V(t_n) < \alpha)$, which simply states that all V_o values up to t_n are below α:

$$\begin{aligned} &P\left(T_\alpha > t_n\right) = P\left(V(t_1) < \alpha, V(t_2) < \alpha, ..., V(t_n) < \alpha\right) \\ &= P\left(V(t_n) < \alpha \mid V(t_{n-1}) < \alpha, ..., V(t_1) < \alpha\right) \times P\left(V(t_{n-1}) < \alpha, ..., V(t_1) < \alpha\right) \\ &= P\left(V(t_n) < \alpha \mid V(t_{n-1}) < \alpha\right) \times P\left(V(t_{n-1}) < \alpha, ..., V(t_1) < \alpha\right) \text{ (Lemma 1)} \\ &= P\left(V(t_n) < \alpha \mid V(t_{n-1}) < \alpha\right) \times P\left(V(t_{n-1}) < \alpha \mid V(t_{n-2}) < \alpha, ..., V(t_1) < \alpha\right) \\ &\quad \times P\left(V(t_{n-2}) < \alpha, ..., V(t_1) < \alpha\right) \\ &= P\left(V(t_n) < \alpha \mid V(t_{n-1}) < \alpha\right) \times P\left(V(t_{n-1}) < \alpha \mid V(t_{n-2}) < \alpha\right) \times ... \times \\ &\quad P\left(V(t_2) < \alpha \mid V(t_1) < \alpha\right) \times P\left(V(t_1) < \alpha\right) \end{aligned} \quad (10)$$

Using the conditional probability and for $P(V(t_{i-1}) < \alpha) > 0$:

$$P\left(V(t_i) < \alpha \mid V(t_{i-1}) < \alpha\right) = \frac{P\left(V(t_i) < \alpha \wedge V(t_{i-1}) < \alpha\right)}{P\left(V(t_{i-1}) < \alpha\right)} \quad (11)$$

Substituting equation (11) in Equation produces the desired result and concludes the proof. ■

Equation (9) enables us to calculate the distribution of any $\alpha\%$ crossing time of the output voltage. The remainder of this section focuses on the calculation of probability in Equation (11). The term $P(V(t_i) < \alpha)$ for $1 \le i \le n$ can be directly calculated from the probability distribution of the voltage at each time instance.

***Definition* 2**: The bivariate normal distribution is given by:

$$P(x_1, x_2) = \frac{1}{2\pi\sigma_1\sigma_2\sqrt{1-\rho^2}} \exp\left[-\frac{z}{2(1-\rho^2)}\right]$$

$$\text{where } z = \frac{(x_1-\mu_1)^2}{\sigma_1} - \frac{2\rho(x_1-\mu_1)(x_2-\mu_2)}{\sigma_1\sigma_2} + \frac{(x_2-\mu_2)^2}{\sigma_2^2} \quad (12)$$

$$\rho = corr(X_1, X_2) = \frac{\sigma_{12}}{\sigma_1 \cdot \sigma_2} \text{ and } \sigma_{12} = \text{cov}(X_1, X_2)$$

The distribution of the $V_o(t_i)$ and $V_o(t_{i-1})$ are correlated normal distributions (because each is a weighted linear summation of the normal distributions associated with the process.) In order to calculate the joint probability of $V_o(t_i)$ and $V_o(t_{i-1})$ from Equation (12), the following lemma is applied to find their covariance.

***Lemma* 2:** Suppose that the distribution of the voltage values at times t_i and t_{i-1} is given in first-order form as follows:

$$V_o(t_i) = a_0 + \sum_{i=1}^{m} a_i \cdot \Delta X_i \; ; \; V_o(t_{i-1}) = b_0 + \sum_{i=1}^{m} b_i \cdot \Delta X_i \quad (13)$$

where m is the number of sources of variation. ΔX_i's are normalized to $N(0,1)$ by appropriate coefficient scaling. The covariance of $V_o(t_i)$ and $V_o(t_{i-1})$ can be calculated as follows:

$$\begin{aligned} &\sigma_{12} = \text{cov}\left(V_o(t_i), V_o(t_{i-1})\right) = E\left((V_o(t_i) - E(V_o(t_i))) \times (V_o(t_{i-1}) - E(V_o(t_{i-1})))\right) \\ &= E\left((\sum_{i=1}^{m} a_i \cdot \Delta X_i) \times (\sum_{i=1}^{m} b_i \cdot X_i)\right) = E\left(\sum_{i=1}^{m} a_i b_i \Delta X_i^2\right) + E\left(\sum_{i=1}^{m} \sum_{j<i} a_i b_j \Delta X_i \Delta X_j\right) \\ &= \sum_{i=1}^{m} a_i b_i \quad \text{because } E\left(\Delta X_i^2\right) = 1 \text{ and } E\left(\Delta X_i \Delta X_j\right) = E\left(\Delta X_i\right) \times E\left(\Delta X_j\right) = 0. \end{aligned}$$

Equation (9) along with definition 2 and lemma 2 provide complete information for computing the probability distribution of any $\alpha\%$ crossing time of the output voltage.

It is possible to encounter multiple $\alpha\%$ crossing times. The procedure explained above can be used to iteratively find all $\alpha\%$ crossing times. More precisely, after the first $\alpha\%$ crossing, a new Markovian process is considered that starts from this hitting time. Assuming low to high transition for the output voltage, the waveform reaches the second hitting time from a higher voltage than α. The event $(T_\alpha > t_n)$ is thus equivalent to the event $(V(t_1) > \alpha \wedge V(t_2) > \alpha \wedge ... \wedge V(t_n) > \alpha)$. Equation (9) can be easily modified to calculate the distribution of the second hitting time for the new process, and so on.

It can be shown that, for known and small number of sources of variation, the algorithm complexity is $O(n \times k^2)$ where the pdf of the output voltage at each time instance is discretized with k sample points.

4. Experimental Results

To evaluate the proposed current-based modeling approach, it was compared with Hspice [9]. The set of experiments involved various logic cells, including simple inverter and NAND gates, as well as complex cells such as AOI (And-Or-Invert).

Figure 3 shows comparison with Hspice for some examples of crosstalk-induced noisy waveforms given to a minimum size inverter in 130nm cell library. The equivalent output waveforms generated by our model match the Hspice results closely.

Next comparison with the KTV model [2] is presented. Figure 4 illustrates the absolute delay errors w.r.t. to Hspice for a minimum size inverter in our 130nm cell library. The input line to the inverter is coupled by a 50fF capacitance and is under attack by an aggressor line. Both the victim and aggressor are driven by minimum size inverters. The cell under consideration has a FO4 load. The signal arrival time of the input of the victim line driver is set to 10ps while that of the aggressor (i.e., the noise injection time) is swept from

100ps to 200ps with a time step of 1ps. Compared to KTV, the accuracy of delay calculation for the minimum size inverter is improved by 8.8% (17.3%) on average (max), respectively. Figure 5 shows the absolute delay error trend for a similar experiment performed on AOI22 cell with size 10x. The coupling value is 80fF. The accuracy improvement in this case is 52.1% (93.4%) on average (max.)

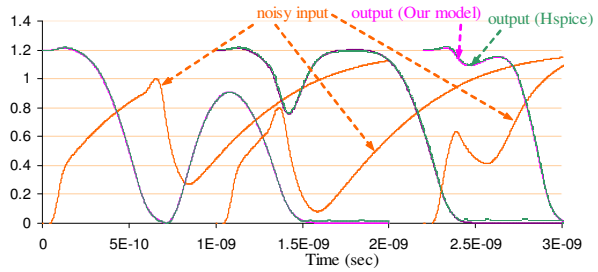

Figure 3. The actual and equivalent waveforms by our model for some crosstalk-induced noisy waveforms.

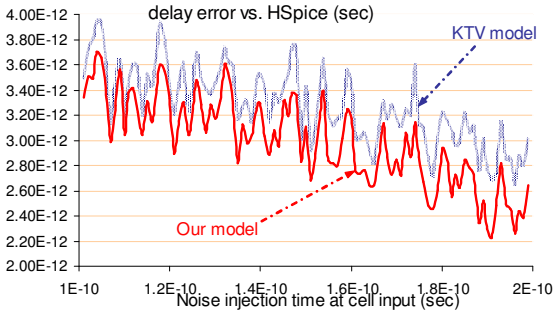

Figure 4. Absolute errors in calculated delay for a min size inverter

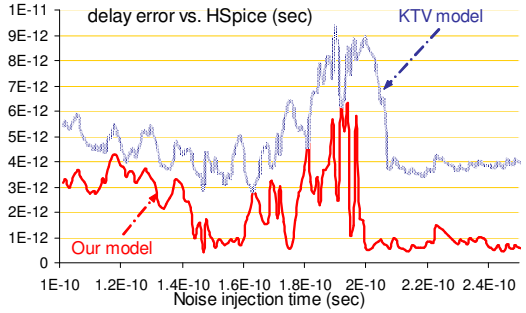

Figure 5. Absolute errors in calculated delay for an AOI22 size 10x.

As discussed earlier, the shape of the waveform greatly impacts the delay calculation, therefore, delay and output slew metrics may not be sufficient to model the waveform shape. Our current-based model is capable of producing output waveforms whose shapes are very close to those produced by Hspice. Mean square error (MSE) is a good metric to compare waveform shapes. Figure 6 shows MSE for our cell model and KTV compared to Hspice. It is seen that this value is lower for our model compared to KTV in most of the cases. In fact, the average MSE improvement for the inverter (AOI22) for the aforementioned experiment setup is 11.3% (24.5%.)

Next, we evaluate our statistical analysis methodology in handling the effect of the process variations on cell output waveform and, more specifically, the cell delay. We performed extensive Hspice based Monte-Carlo simulations to calculate the 50% cell delay distribution over our test-cases, namely, the minimum size inverter as well as the AOI22 cell with the same experimental setup explained before. We assumed 3σ variation of 15% for the sources of variation [10]. We also calculated the delay distribution using the mathematical approach presented in section 3. For each arrival time of the aggressor (noise injection time) we compared the mean and the variance of the 50% delay computed by our proposed mathematical approach and that of Monte-Carlo simulation. The average and maximum error results over all noise injection times are reported in Table 1.

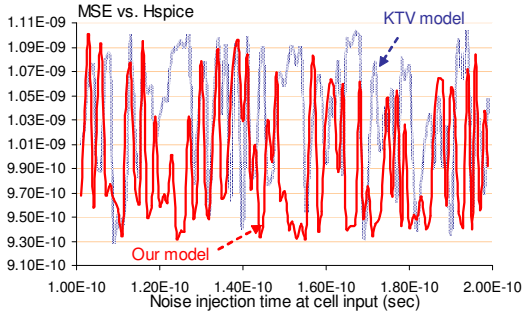

Figure 6. Waveform similarity (mean square error) comparison to Hspice for our model and the KTV model.

Table 1: Average and maximum percentage error by our mathematical method and Monte-Carlo.

Error %	Mean		Variance	
	Avg error	Max error	Avg error	Max error
Inverter	1.1%	3.9%	1.5%	4.4%
AOI22	1.4%	4.5%	1.7%	4.9%

5. Conclusions

A statistical logic cell delay model for the purpose of cell timing analysis was presented. A new current-based cell delay model was developed to accurately capture various cell parasitic and nonlinear effects in the computation of output voltage waveform in the presence of crosstalk-induced noise. A novel statistical analysis methodology was also presented to capture the effect of process variations on the cell output waveform. The cell output voltage waveform was modeled by a Markovian stochastic process. Consequently the distribution of cell timing parameters such as α% crossing time was computed. Experimental results showed the high accuracy of our cell delay model compared to the existing cell delay models. Comparison with Monte-Carlo-based SPICE simulations shows the high accuracy of the presented mathematical approach in dealing with process variations.

References

[1] J.F. Croix, D.F. Wong, "Blade and razor: cell and interconnect delay analysis using current-based models," *Proc. DAC*, pp. 386-389, 2003.

[2] I. Keller, K. Tseng, N. Verghese, "A robust cell-level crosstalk delay change analysis," *Proc. ICCAD*, pp.147-154, 2004.

[3] K. Okada, K. Yamaoka, H. Onodera, "A statistical gate-delay model considering intra-gate variability," *Proc. ICCAD*, pp. 908-913, 2003.

[4] A.Agarwal, F.Dartu, D.Blaauw, "Statistical gate delay model considering multiple input switching," *Proc. DAC*, pp. 658-663, 2004.

[5] C.Visweswariah, K.Ravindran, K.Kalafala, S.G.Walker, S. Narayan, "First-order incremental block-based statistical timing analysis," *Proc. DAC*, pp. 331-336, 2004.

[6] H. Chang, V. Zolotov, C. Visweswariah, S. Narayan, "Parameterized Block-Based Statistical Timing Analysis with Non-Gaussian Parameters and Nonlinear Delay Functions," *Proc. DAC*, pp. 71-76, 2005.

[7] H. chang, S. Sapatnekar, "Statistical Timing Analysis Considering Spatial Correlations Using a Single PERT-like Traversal," *Proc. ICCAD*, pp. 621-625, 2003.

[8] G.F. Lawler, *Introduction to Stochastic Process*, Chapman & Hall, 2000.

[9] “Hspice: The golden standard for Accurate Circuit Simulation,” http://www.synopsys.com/products/mixedsignal/hspice/hspice.html.
[10] S. Nassif, “Modeling and Analysis of Manufacturing Variations,” *Proc. CICC*, pp. 223-228, 2001.